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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/882,911 | 06/15/2001 | John A. Michejda | MICHEJDA 4-6 | 9771 |

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| EXAMINER | |
|---|---|
| FENTY, JESSE A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/882,911 | MICHEJDA ET AL. | |
| | Examiner | Art Unit | |
| | Jesse A. Fenty | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 7, 9, 10, 12, 15 and 17-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Subramanian et al. (U.S. Patent No. 5,494,837).

In re claims 1, 9 and 17, Subramanian (Figs. 3A-3L) discloses a semiconductor device and method of forming the same, comprising:

A channel region (C) located in a semiconductor substrate (10);

A trench (24) located adjacent a side of the channel region;

An isolation structure (30) located in the trench (above the trench bottom 24c)[1];

A sidewall spacer (30) located over at least one sidewall (24b) of the trench distal the channel region;

A source/drain (S, D) region located over the isolation structure; and

Dielectric layers (16) located over the semiconductor devices and having interconnect structures (36) located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

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[1] Parenthetical added for clarity. See Response to Arguments for further explanation.

In re claims 2, 10 and 18, Subramanian discloses the devices of claims 1, 9 and 17 respectively, wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure (30) located in the first trench and the semiconductor device further includes a second isolation structure (30) located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor device further includes a second source/drain region located over the second isolation structure.

In re claims 4 and 12, Subramanian discloses the devices of claims 1 and 9 respectively, wherein the source/drain region comprises epitaxial silicon (column 5, lines 44-51).

In re claims 7, 15 and 19, Subramanian discloses the devices of claims 1, 9 and 17 respectively, wherein the isolation structure comprises an oxide (column 5, lines 28-31).

In re claim 20, Subramanian discloses the device of claim 17, wherein the semiconductor devices from part of an NMOS device, a PMOS device (Fig. 5M) or a bipolar device (Fig. 5M).

In re claims 21 and 22, Subramanian discloses the devices of claims 1 and 9 respectively, wherein the sidewall spacer is not contiguous the side of the channel region.

## *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian as applied to claims 1 and 9 above, and further in view of Blanchard (US 2001/0000111 A1).

In re claims 3 and 11, Subramanian discloses the devices of claims 1 and 9 respectively, but does not expressly disclose the source/drain region comprising polysilicon. Blanchard (Fig. 1) discloses source/drain regions comprising polysilicon (109). It would have been obvious for one skilled in the art at the time of the invention to use polysilicon source/drain regions as disclosed by Blanchard for the device of Subramanian for the purpose, for example, eliminating hot carrier effects or improving circuit element density (Blanchard; pp. 3, section [0023, lines 15-17, 21-25)].

5. Claims 5, 6, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian as applied to claims 1 and 9 above, and further in view of Komori et al. (U.S. Patent No. 5,598,019).

In re claims 5, 6, 13 and 14, Subramanian discloses the devices of claims 1 and 9 respectively, but does not expressly disclose an oxide layer located between a nitride sidewall spacer and at least one sidewall of the trench. Komori (Fig. 47) discloses an oxide layer (12) located between a nitride sidewall spacer layer (15) and a trench (10). It would have been obvious to one skilled in the art at the time of the invention to use a multi-layer insulation structure as disclosed by Komori for the device of Subramanian for the purpose, for example, of enhancing the isolation capability and reliability of the device (Komori; column 17, lines 53-58).

6. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian as applied to claims 1 and 9 above, and further in view of Pan (U.S. Patent No. 5,814,863) and Tseng (U.S. Patent No. 5,753,557).

In re claims 8 and 16, Subramanian discloses the devices of claims 1 and 9 respectively, comprising highly doped contact regions (32) but does not expressly disclose the source/drain regions comprising LDD regions. Pan and Tseng disclose semiconductor devices with LDD and highly doped contact regions comprising dopant concentrations ranging from about 1E16 atoms/$cm^3$ to about 1E17 atoms/$cm^3$ and forming highly doped source/drain contact regions having a dopant concentration up to about 1E22 atoms/$cm^3$ (Tseng, column 5, lines 57-64; Pan, column 5, lines 13-18, 30-36). It would have been obvious for one skilled in the art at the time of the invention to form doped regions of Subramanian in the manner disclosed by Pan and Tseng for the purpose, for example, of spreading out the high electric field near the drain junction, allowing the device to be operated at a higher supply voltage with fewer hot-electron problems (column 1, lines 55-63).

***Response to Arguments***

7. Applicant's arguments filed 01/21/04 have been fully considered but they are not persuasive.

a. In re claim 1, Applicant argues that the device of Subramanian et al. ('837) does not anticipate the claimed invention because the isolation layer (30) is used to denote both the isolation structure as well as the sidewall spacer. Examiner avers that this is not

the case. The insulating layer (30) comprises three separate portions, two of which read on the claimed regions:

i. The horizontal portion of the insulating layer (30) atop the bottom of the trench (24c) anticipates the claimed "isolation structure";

ii. The vertical portion of the insulating layer (30) over at least one sidewall (24c) anticipates the claimed "sidewall spacer"; and

iii. The horizontal portion of the insulating layer (30) on the face (10a) of the semiconductor substrate.

In the Non-Final Office Action mailed 11/26/03, Examiner cited the sidewall spacer (30) overlying the sidewall (24b) of the trench distal the channel region. For clarity, a parenthetical noting the distinctness of the two regions has been added to the body of the rejection. This is not a new ground of rejection. Applicant is responsible for interpreting the prior art and comparing such to a broad reading of the submitted claims. The reference clearly discloses two sections of the trench (24b and 24c) that correspond to two sections of the insulating layer (30) in the trench. The prior art anticipates the claimed invention.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

TOM THOMAS
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